

A DEVICE FOR DEBUGGING AND METHOD THEREOF

FIELD OF THE INVENTION

The present invention is related to a device for debugging and method thereof, particularly to a debugging device and method, transparent with operating system.

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BACKGROUND OF THE INVENTION

In the current computer system, system designers usually have some difficulties of hardware and software in designing and debugging motherboard. Generally, the designers solve those problems with debugging engine or software debugging program. For example, logical analyzer (LA) and SCOPES is used to sample working period of PCI and wave pattern of signal and hardware ICE is used to capture the instruction flow of CPU, or software ICE is used to capture the instruction flow of operating system.

10 However, these hardware tools such as LA, SCOPES, hardware ICE, etc. are very expensive, and whose operation procedures are too complicated to meet the demand of users interface.

15 On the other hand, although the costs of debugging by software ICE tool program are not as expensive as hardware tools, they are not cheap, either. And, the usage of software tool program is limited while operating system is starting at the power-on stage; however, some other bugs are still may happen before the system initiated. Furthermore, debugging system by software ICE tool program will change the execution procedure from operating system that would cause other unpredictable bugs. This is why the usage of software ICE tool program is not an effective choice.

20 Thus, the main purpose of present invention is to develop an effective and low cost debugging tool that makes system design more convenient and the debugging procedure simpler.

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SUMMARY OF THE INVENTION

Accordingly, it is therefore a primary object of the present invention to provide a device for debugging and method thereof, providing a debugging tool

program stored in the system management mode section of basic input output system (BIOS). The debugging tool program could be triggered by system management interrupt signal to achieve the purpose of debugging at any time.

5 A secondary object of the present invention is to provide a device for debugging and method thereof, displaying the debugging operation window from the debugging tool program, for selecting and executing each debugging item to achieve the purpose of simple and convenient operation.

10 Another object of the present invention is to provide a device for debugging and method thereof, transparent with CPU to reduce other bugs caused during the debugging procedure.

15 Therefore, for achieving aforementioned objects, the primary method according to one preferred embodiment of the present invention includes a method for debugging, presented in a computer system, wherein the computer system includes a CPU connected to a chipset with system management interrupt pin, the method thereof comprising steps of sending a system management interrupt signal to CPU through the system management interrupt pin of chipset; the CPU move into a system management mode and execute popping out a debugging operation window for selecting and executing each debugging item; and after the execution 20 of the debugging procedure completing, leaving the debugging operation window and returning to the next instruction before debugging.

25 For achieving aforementioned objects, the primary structure according to one preferred embodiment of the present invention includes a CPU connected to at least one memory and a chipset with at least one system management interrupt pin to connect with CPU; a system management mode section provided in the memory; and a debugging tool program displayed from a debugging operation window provided inside the system management mode section.

BRIEF DESCRIPTION OF THE DRAWINGS

30 The objects, spirits and advantages of the preferred embodiments of the present invention will be readily understood by the accompanying drawings and detailed descriptions, wherein:

Figure 1 is a block diagram of a device for debugging according to one preferred embodiment of the present invention;

Figure 2 is a flow diagram of a method for debugging according to one preferred embodiment of the present invention; and

5 Figure 3 is a schematic diagram of the debugging operation of the present invention transparent with the operating system.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The structural features and the effects to be achieved may further be understood and appreciated by reference to the presently preferred embodiments
10 together with the detailed description.

The current Central Processing Unit (CPU), such as Intel Pentium 4 and AMD K8, both provide system management mode (SMM) for users to control the system management by a firmware, such as BIOS, and the system management mode is transparent with operating system (OS). The system management mode
15 could be triggered by a system management interrupt signal (SMI#). The system management interrupt is generated by system management interrupt signal through SMI# pin for Intel P4 CPU, or SMI# message for AMD K8 CPU. When the CPU receives the system management interrupt signal, it moves into the system management mode for executing the predetermined program, which is stored in the system management mode section. After end of execution, the CPU
20 will leave the system management mode and return to OS by a resume instruction (RSM). According to this characteristic, the present invention provides a debugging tool program stored in the system management mode section of BIOS for the operation of users.

25 Firstly, referring to Figures 1 and 2, there are a block diagram of debugging device and a flow chart of debugging method, respectively, according to one preferred embodiment of the present invention. As shown in these figures, the computer system includes a CPU 10 connected to a north-bridge chipset 12 through the link 13. The north-bridge chipset 12 connected to a south-bridge
30 chipset 14 through the link 15. The south-bridge chipset 14 is connected to the CPU through SMI# pin 16 and includes a plurality of general purpose input/output (GPIO) pins. As debugging, users have to select the GPIO pin 18 of the

south-bridge chipset 14 and trigger the south-bridge chipset 14 to send a system management interrupt signal. As shown in step 20, the users trigger the south-bridge chipset 14 to send a system management interrupt signal through the predetermined GPIO pin 18. As shown in step 22, as the CPU receives the system 5 management interrupt signal through SMI# pin 16, or SMI# message through the Links 13 and 15 between chipsets, it will move into the system management mode, provided in a section of BIOS of DRAM, such that the system management mode section is provided in the BIOS and a predetermined debugging tool program is provided in the system management mode section. Thus, the debugging tool 10 program will be triggered when CPU 10 moves into the system management mode as shown in step 24. The debugging tool program provides users a debugging operation window for operating and selecting each debugging item that includes access input/output, access memory, access device configuration and trap set for specific IO address as shown in step 26. Finally, after completing the operation 15 and leaving the debugging operation window, the CPU will return to the original procedure to execute the next queued instruction (referring to Figure 3), as shown in step 28.

Referring to Figure 3, which is the schematic diagram of the debugging operation of the present invention transparent with the operating system. When the 20 CPU executes procedure 30, the system management interrupt signal is triggered by users in instruction n. And when the execution of debugging tool program 32 is completed, the system will return to the instruction n+1 of procedure 30, to continue the execution of original procedure. Thus, the execution of original OS procedure will not be influenced, and reduce the possible bugs caused from 25 debugging execution by the debugging tool program.

Certainly, even the execution of debugging is completed, the system management interrupt signal could be triggered by users at any time to execute 30 debugging tool program again. Otherwise, if users have already set a trap address during the debugging procedure, then the system management interrupt signal would be triggered to pop out debugging operation window for users to debug when CPU is processing to the trap address, as to repeat from step 22 to step 28.

Since the debugging tool program is provided in the BIOS, it won't increase any the cost of product. Besides, the debugging operation window is programmable to provide more convenient advantage for users. Furthermore, it is transparent with the OS for reducing other possible bugs. The present invention is
5 the effective method to solve the difficulties of high cost and low efficiency of debugging

The device for debugging and method disclosed in the present invention has the SMI to trigger the debugging operation window, in order to execute each debugging item. Therefore the system design becomes easier, and the debugging
10 procedure becomes simpler, which result in the purpose of being more effective and lower cost.

Although this invention has been disclosed and illustrated with reference to particular embodiments, the principles involved are susceptible for use in numerous other embodiments that will be apparent to persons skilled in the art. This invention is,
15 therefore, to be limited only as indicated by the scope of the appended claims.

LIST OF REFERENCE SYMBOLS

10	Central Processing Unit
12	north-bridge Chipset
14	south-bridge Chipset
5 16	circuit

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